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| TRANSMITTAL FORM <i>(to be used for all correspondence after initial filing)</i> | | Application No. | 10/671,844 |
| | | Filing Date | September 25, 2003 |
| | | First Named Inventor | Sujat Jamil |
| | | Art Unit | 2183 |
| | | Examiner Name | Fiegle, Ryan Paul |
| Total Number of Pages in This Submission | 3 | Attorney Docket Number | 42P17407 |

| ENCLOSURES (check all that apply) | | |
|--|---|--|
| <input checked="" type="checkbox"/> Fee Transmittal Form <input type="checkbox"/> Fee Attached <input type="checkbox"/> Amendment / Response <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declaration(s) <input type="checkbox"/> Extension of Time Request <input type="checkbox"/> Express Abandonment Request <input type="checkbox"/> Information Disclosure Statement <input type="checkbox"/> PTO/SB/08 <input type="checkbox"/> Certified Copy of Priority Document(s) <input type="checkbox"/> Response to Missing Parts/Incomplete Application <input type="checkbox"/> Basic Filing Fee <input type="checkbox"/> Declaration/POA <input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53 | <input type="checkbox"/> Drawing(s) <input type="checkbox"/> Licensing-related Papers <input type="checkbox"/> Petition <input type="checkbox"/> Petition to Convert a Provisional Application <input type="checkbox"/> Power of Attorney, Revocation Change of Correspondence Address <input type="checkbox"/> Terminal Disclaimer <input type="checkbox"/> Request for Refund <input type="checkbox"/> CD, Number of CD(s) <input type="checkbox"/> Landscape Table on CD | <input type="checkbox"/> After Allowance Communication to TC <input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences <input type="checkbox"/> Appeal Communication to TC (Appeal Notice, Brief, Reply Brief) <input type="checkbox"/> Proprietary Information <input type="checkbox"/> Status Letter <input checked="" type="checkbox"/> Other Enclosure(s) (please identify below): <div style="border: 1px solid black; padding: 5px; margin-top: 10px;">Please see Remarks:</div> |
| Remarks Request for Original Filing Date; Statement of Attestation; Response mailed on 04/10/2006 and related transmittals; and Return receipt postcard. | | |

| SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT | |
|--|---|
| Firm or Individual name | Joseph Lutz, Reg. No. 43,765 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP |
| Signature | |
| Date | September 26, 2006 |

| CERTIFICATE OF MAILING/TRANSMISSION | | | |
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| Typed or printed name | | Annie McNally | |
| Signature | | Date | 09/26/2006 |

Based on PTO/SB/21 (09-04) as modified by Blakely, Solokoff, Taylor & Zafman (wlr) 11/30/2005.
SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450



Attorney's Docket No. 042390.P17407

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application for:

Sujat Jamil et al.

Application No.: 10/671,844

Filed: September 25, 2003

For: APPARATUS AND METHOD FOR
POWER OPTIMIZED REPLAY

Examiner: Fiegler, Ryan Paul

Art Unit: 2183

Mail Stop Amendment
Commissioner for Patents
Post Office Box 1450
Alexandria, Virginia 22313-1450

STATEMENT OF ATTESTATION UNDER C.F.R. §1.8 (b)(3)

I, Marilyn Bass, under the penalty of perjury, declare that I personally mailed the above-mentioned Amendment and Response Office Action on April 10, 2006 by first-class U.S. mail.

Date: Sep. 26, 2006

Marilyn Bass
Marilyn Bass

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Annie McNally
Annie McNally

09/26/2006
Date



Attorney's Docket No. 042390.P17407

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In re Application for:

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Application No.:
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Filed: September 25, 2003

For: APPARATUS AND METHOD FOR
POWER OPTIMIZED REPLAY

Examiner: Fiegler, Ryan Paul

Art Unit: 2185

Mail Stop Amendment
Commissioner for Patents
Post Office Box 1450
Alexandria, Virginia 22313-1450

REQUEST FOR ORIGINAL FILING DATE UNDER 37 C.F.R. § 1.8 (b)

This resubmission, under 37 C.F.R. § 1.8 (b), is to request the original mailing date of Amendment and Response, mailed April 10, 2006, to the Office Action mailed January 10, 2006. Enclosed is a copy of the Amendment and Response to Office Action, as filed, including a certificate of mailing. Also enclosed are a copy of check no. 002229 and the fee transmittal that accompanied the response when filed.

A return postcard has not been received and no indication of a receipt of the response was found in the PAIR system. Please find attached a Statement of Attestation under 37 C.F.R. § 1.8(b)(3) from the individual responsible for mailing the above mentioned document and who signed the original certificate of mailing.


Please charge all the appropriate fees to Deposit Account No. 02-2666. A copy of the Fee Transmittal is enclosed for deposit account charging purposes.

If you have any questions please contact me at (310) 500-4767.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: Sep. 26, 2006

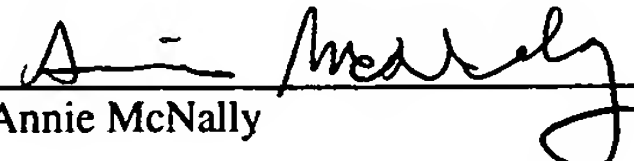


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 09/26/2006
Annie McNally Date



TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

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| Application No. | 10/671,844 | | |
| | Filing Date | September 25, 2003 | |
| | First Named Inventor | Sujat Jamil | |
| | Art Unit | 2183 | |
| | Examiner Name | Fiegle, Ryan Paul | |
| Total Number of Pages in This Submission | 19 | Attorney Docket Number | 42P17407 |

ENCLOSURES (check all that apply)

☒ Fee Transmittal Form

☒ Fee Attached

☒ Amendment / Response

☐ After Final

☐ Affidavits/declaration(s)

☐ Extension of Time Request

☐ Express Abandonment Request

☐ Information Disclosure Statement

☐ PTO/SB/08

☐ Certified Copy of Priority Document(s)

☐ Response to Missing Parts/Incomplete Application

☐ Basic Filing Fee

☐ Declaration/POA

☐ Response to Missing Parts under 37 CFR 1.52 or 1.53

☐ Drawing(s)

☐ Licensing-related Papers

☐ Petition

☐ Petition to Convert a Provisional Application

☐ Power of Attorney, Revocation Change of Correspondence Address

☐ Terminal Disclaimer

☐ Request for Refund

☐ CD, Number of CD(s)

☐ Landscape Table on CD

☐ After Allowance Communication to TC

☐ Appeal Communication to Board of Appeals and Interferences

☐ Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)

☐ Proprietary Information

☐ Status Letter

☒ Other Enclosure(s) (please identify below):

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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

| | |
|--------------------------------|--|
| Firm or Individual name | Joseph Lutz, Reg. No. 43,765 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP |
| Signature | |
| Date | April 10, 2006 |

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| | | | |
|------------------------------|--------------|-------------|----------------|
| Typed or printed name | Marilyn Bass | | |
| Signature | | Date | April 10, 2006 |



Attorney's Docket No. 42P17407

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Sujat Jamil et al.

Application No. 10/671,844

Filed: September 25, 2003

For: **APPARATUS AND METHOD FOR
POWER OPTIMIZED REPLAY**

Examiner: Fiegle, Ryan Paul

Art Unit: 2183

AMENDMENT AND RESPONSE TO OFFICE ACTION

Mail Stop Amendment
Commissioner for Patents
P. O. 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action mailed January 10, 2006, Applicants respectfully request entry of the following amendments and seek reconsideration in view of the following remarks.

A circular black ink stamp. The text "OIP" is at the top, "IAP" is at the top right, "SEP 29 2006" is in the center, and "PATENT & TRADEMARK OFFICE" is at the bottom.

☐ Check No. 1001 in the Amount of \$100.00

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN, LLP

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April 10, 2006

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IN THE SPECIFICATION

Please amend the specification as follows:

Beginning on page 6, ¶00028:

[00028] Unfortunately, as indicated, uOPs within the system pipeline may encounter situations known as hazards where subsequent uOPs cannot execute until completion of a previous uOP. Examples include data hazards where a subsequent uOP needs to view the side effects of a previous uOP in order to execute. A further example is resource hazards where the later uOP ~~need~~needs to use a resource that continues to be occupied by an earlier uOP. Collectively, the various hazards described herein are referred to as “instruction blocking condition(s)”. Conventionally, hazard situations are handled by using a technique referred to as “stalling”, which includes various drawbacks.

On page 15, ¶00056:

[00056] In any representation of the design, the data may be stored in any form of a machine readable medium. ~~An optical or electrical wave 660 modulated or otherwise generated to transport such information, a~~ memory 650 or a magnetic or optical storage 640, such as a disk, may be the machine readable medium. Any of these mediums may carry the design information. The term “carry” (e.g., a machine readable medium carrying information) thus covers information stored on a storage device ~~or information encoded or modulated into or onto a carrier wave~~. The set of bits describing the design or a particular of the design are (when embodied in a machine readable medium, such as a ~~carrier or~~ storage medium) an article that may be sealed in and out of itself, or used by others for further design or fabrication.

IN THE CLAIMS

1. (Currently Amended) A method comprising:
issuing an instruction selected from a queue;
enqueueing the instruction issued within a recirculation queue in one of a blocked state and an unblocked state if completion of the instruction is prevented by a detected blocking condition; and
reissuing a selected instruction from the recirculation queue ~~once~~ if a detected blocking condition of ~~an~~ at least one instruction within the recirculation queue, other than the selected instruction, is satisfied.
2. (Original) The method of claim 1, wherein issuing comprises:
arbitrating between a plurality of queues to select a queue;
selecting a current instruction from the queue selected; and
issuing the current instruction for the queue selected.
3. (Original) The method of claim 2, wherein issuing the current instruction comprises:
determining a state of the current instruction;
selecting an alternate queue from the plurality of queues if a state of the selected instruction is blocked; and
issuing an instruction selected from the alternate selected queue.
4. (Original) The method of claim 1, wherein enqueueing comprises:
detecting the blocking condition prohibiting the instruction issued from completion;
placing the instruction within the recirculation queue;
setting a state of the instruction as blocked to prohibit reissue of the instruction; and
storing the detected blocking condition.
5. (Original) The method of claim 1, further comprising:
identifying blocking conditions of instructions within the recirculation queue;

determining whether any blocking condition of any instruction within the recirculation queue is satisfied;

enabling recirculation of instructions from the recirculation queue by setting a state of each instruction within the recirculation queue to an unblocked state if any blocking condition is satisfied.

6. (Original) The method of claim 1, wherein reissuing instructions comprises:
receiving a request to issue an instruction contained within the recirculation queue;
determining a state of a current instruction of the recirculation queue;
issuing the current instruction if the state of the current instruction is an unblocked state in response to the received request; and
disregarding the request if the state of the current instruction is a blocked state.

7. (Original) The method of claim 1, wherein enqueueing comprises:
determining whether the detected blocking condition preventing the instruction issued from completion is a transient blocking condition;
setting a state of the instruction to an unblocked state if the detected blocking condition is transient; and
resetting a state of each instruction within the recirculation queue to an unblocked state.

8. (Original) The method of claim 1, wherein reissuing selected instructions comprises:
issuing an unblocked instruction in response to a received request;
enqueueing the reissued instruction if a blocking condition of the instruction remains unsatisfied;
setting a state of the reissued instruction to a blocked state; and
storing the blocking condition.

9. (Original) The method of claim 1, wherein the detected blocking condition is one of a data blocking condition and a resource blocking condition.

10. (Original) The method of claim 1, wherein the recirculation queue is a first in, first out circular queue.

11. (Currently Amended) An article of manufacture including a machine readable medium having stored thereon instructions which may be used to program a system to perform a method, comprising:

issuing an instruction selected from a queue;

enqueueing the instruction issued within a recirculation queue in one of a blocked state and an unblocked state if completion of the instruction is prevented by a detected blocking condition; and

reissuing a selected instructions from the recirculation queue ~~once~~ if a detected blocking condition of ~~an~~ at least one instruction within the recirculation queue, other than the selected instruction, is satisfied.

12. (Original) The article of manufacture of claim 11, wherein issuing comprises: arbitrating between a plurality of queues to select a queue; selecting a current instruction from the queue selected; and issuing the current instruction from the queue selected.

13. (Original) The article of manufacture of claim 12, wherein issuing comprises: determining a state of the current instruction; selecting an alternate queue from the plurality of queues if a state of the selected instruction is blocked; and issuing an instruction selected from the alternate selected queue

14. (Original) The article of manufacture of claim 11, wherein enqueueing comprises: detecting the blocking condition prohibiting the instruction issued from completion; placing the instruction within the recirculation queue; setting a state of the instruction as blocked to prohibit reissue of the instruction; and storing the detected blocking condition.

15. (Original) The article of manufacture of claim 11, wherein the method further comprises:

- identifying blocking conditions of instructions within the recirculation queue;
- determining whether any blocking condition of any instruction within the recirculation queue is satisfied;

- enabling reissuing of instructions from the recirculation queue by setting a state of each instruction within the recirculation queue to an unblocked state if any blocking condition is satisfied.

16. (Original) The article of manufacture of claim 11, wherein reissuing selected instructions comprises:

- receiving a request to issue an instruction contained within the recirculation queue;
- determining a state of a current instruction of the recirculation queue;
- issuing a current instruction if the state of the current instruction is an unblocked state;

and

- disregarding the request if the state of the current instruction is a blocked state.

17. (Original) The article of manufacture of claim 11, wherein enqueueing comprises:

- determining whether the detected blocking condition preventing the instruction issued from completion is a transient blocking condition;

- setting a state of the instruction to an unblocked state if the detected blocking condition is transient; and

- resetting a state of each instruction within the recirculation queue to an unblocked state.

18. (Original) The article of manufacture of claim 11, wherein reissuing selected instructions comprises:

- issuing an unblocked instruction in response to a received request;
- enqueueing the reissued instruction if a blocking condition of the instruction remains unsatisfied;

- setting a state of the reissued instruction to a blocked state; and
- storing the blocking condition.

19. (Original) The article of manufacture of claim 11, wherein the detected block condition is one of a data blocking condition and a resource blocking condition.

20. (Original) The article of manufacture of claim 12, wherein the recirculation queue is a first in, first out circular queue.

21. (Currently Amended) An apparatus, comprising:
a received instruction queue to store received instructions;
a recirculation queue;
arbitration logic to select one of the received instruction queue and the recirculation queue from which to issue a current instruction; and
blocked instruction detection logic to identify instructions blocked from execution by detected blocking conditions, and to enqueue the instructions onto the recirculation queue in one of a blocked state and an unblocked state, including a respective blocking condition of each instruction within the recirculation queue, wherein instructions having a transient blocking condition are enqueued onto the recirculation queue in the unblocked state.

22. (Original) The apparatus of claim 21, wherein the blocked instruction detect logic further comprises:

blocked condition satisfaction logic to detect whether a blocking condition of an instruction within the recirculation queue is satisfied and to set a state of each instruction within the recirculation queue to an unblocked state if a blocking condition of an instruction within the recirculation queue is satisfied.

23. (Original) The apparatus of claim 21, wherein the arbitration logic to determine a state of a selected instruction, select the received instruction queue if a state of the selected instruction is blocked, and issue an instruction selected from the received instruction queue.

24. (Original) The apparatus of claim 21, wherein the blocked instruction detect logic to determine whether the detected blocking condition is a transient blocking condition, set a state of the instruction placed within the queue to an unblocked state if the detected blocking

condition is transient, and reset a state of each instruction within the recirculation queue to an unblocked state to enable reissue of instructions contained within the recirculation queue.

25. (Original) The apparatus of claim 21, wherein the blocked instruction detect logic to enqueue a reissued instruction if a blocking condition of the instruction remains unsatisfied, to set a state of the reissued instruction to a blocked state and to store the blocking condition.

26. (Currently Amended) A system comprising:

a memory controller coupled to a memory;

a processor coupled to the memory via a bus, the processor including:

a bus interface unit coupling an execution core to a cache memory including:

a received instruction queue to store received instructions,

a recirculation queue,

arbitration logic to select one of the received instruction queue and the recirculation queue from which to issue a current instruction, and

blocked instruction detection logic to identify instructions blocked from execution by detected blocking conditions, and to enqueue the instructions onto the recirculation queue in one of a blocked state and an unblocked state, including a respective blocking condition of each instruction within the recirculation queue, wherein instructions having a transient blocking condition are enqueued onto the recirculation queue in the unblocked state.

27. (Original) The system of claim 26, wherein the blocked instruction detect logic further comprises:

blocked condition satisfaction logic to detect whether a blocking condition of an instruction within the recirculation queue is satisfied and to set a state of each instruction within the recirculation queue to an unblocked state if a blocking condition of an instruction within the recirculation queue is satisfied.

28. (Original) The system of claim 26, wherein the arbitration logic to determine a state of a selected instruction, select the received instruction queues if a state of the selected instruction is blocked, and issue an instruction selected from the received instruction queue.

29. (Original) The system of claim 26, wherein the blocked instruction detect logic to determine whether the detected blocking condition is a transient blocking condition, set a state of the instruction placed within the queue to an unblocked state if the detected blocking condition is transient, and reset a state of each instruction within the recirculation queue to an unblocked state to enable reissue of instructions contained within the recirculation queue.

30. (Original) The system of claim 26, wherein the blocked instruction detect logic to enqueue the reissued instruction if a blocking condition of the instruction remains unsatisfied, to set a state of the reissued instruction to a blocked state and to store the blocking condition.

Please add the following new claim:

-- 31. (New) The method comprising:

issuing an instruction selected from a queue;

enqueueing the instruction issued within a recirculation queue in one of a blocked state and an unblocked state if completion of the instruction is prevented by a detected blocking condition;

resetting a state of at least one selected instruction within the recirculation queue if a detected blocking condition of at least one instruction within the recirculation queue, other than the at least one selected instruction, is satisfied; and

reissuing a current instruction from the recirculation queue if a state of the current instruction is indicated as the unblocked state. --

REMARKS

In the Office Action, Claims 1-30 were examined and are rejected. In response to the Office Action, Claims 1, 11, 21 and 26 are amended, no claims are cancelled and Claim 31 is added. Applicants respectfully request reconsideration of pending Claims 1-31 in view of the following remarks.

I. Claims Rejected Under 35 U.S.C. §101

The Examiner rejects Claims 11-20 under 35 U.S.C. §101, because the claimed invention is directed to non-statutory subject matter. Applicants respectfully traverse this rejection.

Applicants have amended the specification to delete propagated signals as a machine readable memory.

In view of Applicants' amendments to the specification, Applicants respectfully request that the Examiner withdraw the rejection of Claims 11-20 under 35 U.S.C. §101 as lacking patentable utility.

II. Claims Rejected Under 35 U.S.C. §102

The Examiner rejects Claims 1-9, 11-19 and 21-30 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,395,715 to Merchant et al. ("Merchant"). Applicants respectfully traverse this rejection.

Regarding Claim 1, Claim 1 is amended to recite the following claim features, which are neither disclosed nor suggested by Merchant or the references of record:

enqueueing the instruction issued within a recirculation queue in one of a blocked state and an unblocked state if completion of the instruction is prevented by a detected blocking condition; and

reissuing a selected instruction from the recirculation queue if a detected blocking condition of at least one instruction within the recirculation queue, other than the selected instruction, is satisfied. (Emphasis added.)

According to the Examiner, the above-recited features of Claim 1, prior to amendment, are disclosed by Merchant, and specifically, col. 8, lines 42-53 of Merchant. (See, pg. 3, item 5 of the Office Action mailed January 10, 2006.)

In contrast to the above-recited features of amended Claim 1, Merchant explicitly requires that a long latency instruction may not be re-executed until the condition causing the instruction to not complete successfully is cleared. As explicitly recited by Merchant:

When the condition causing the instruction to not complete successfully is cleared (e.g., when the data returns from the external bus after a cache miss or after completion of a division or multiplication operation or completion of another long latency instruction), the replay queue 170 is then unloaded so that that long latency instruction and the others stored in replay queue 170 may then be re-executed (replayed). (col. 8, lines 46-53.) (Emphasis added.)

Based on the cited passage and as explicitly recited by Merchant, Merchant provides an advantageous solution to allowing non-dependent instructions to execute in parallel while a long latency instruction awaits return of data. To solve this problem, Merchant explicitly discloses the following solution to the problem:

temporarily store the long latency instruction in a replay queue 170 along with its dependent instructions. When the data for the long latency instruction returns from the external memory device, the long latency instruction and its dependent instructions can then be unloaded from the replay queue 170 and sent to mux 116 for replay. In this manner, the long latency instruction will typically not “clog” or unnecessarily delay execution of other non-dependent instructions. (col. 8, lines 14-22.) (Emphasis added.)

Accordingly, based on the cited passages above, the storage of a long latency instruction within the replay queue 170, along with its dependent instructions, results in the storage of the long latency instruction and its respective dependent instructions until the condition causing the instruction to not complete successfully is cleared. Conversely, as recited by amended Claim 1, a selected instruction from the recirculation queue is reissued if a detected blocking condition of at least one instruction within the recirculation queue, other than the selected instruction, is satisfied.

As mandated by case law, “Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim.” Lindemann Maschinenfabrik v. American Hoist & Derrick (“Lindemann”), 730 F.2d 452, 1458 (Fed. Cir. 1994)(emphasis added). Additionally, each and every element of the claim must be exactly disclosed in the anticipatory reference. Titanium Metals Corp. of American v. Banner (“Banner Titanium”), 778 F.2d 775, 777 (Fed. Cir. 1985).

Here, the disclosure in Merchant is expressly limited to the storage of long latency instructions within a replay queue along with instructions dependent from the long latency instruction until a condition causing the long latency instruction not to complete is successfully cleared. (See, supra.) As indicated by Merchant, once the condition is cleared, the long latency

instruction and its dependent instructions can then be unloaded from the replay queue 170 for re-execution. (*See, supra.*)

Hence, the long latency instruction is not reissued until the block condition is satisfied. Furthermore, dependent instructions from the long latency instruction that are stored in the replay queue are not reissued until the long latency instruction is reissued.

Conversely, as recited by amended Claim 1, a selected instruction from a recirculation queue may be reissued if a blocking condition of at least one instruction within the recirculation queue, other than the selected instruction, is satisfied. Applicants respectfully submit that the storage of a long latency instruction within the replay queue, along with its dependent instructions until the condition causing the long latency instruction not to complete successfully is cleared, as disclosed by Merchant, neither discloses, teaches or suggests the above-recited features of amended Claim 1.

Accordingly, Applicants respectfully submit that the Examiner is prohibited from relying on Merchant as an anticipatory reference since Merchant fails to exactly disclose each and every element recited by amended Claim 1 and specifically, the reissue of a selected instruction from a recirculation queue if a detected blocking condition of at least one instruction within the circulation queue, other than the selected instruction, is satisfied. Banner Titanium, supra.

Consequently, Applicants respectfully submit that the Examiner fails to establish a *prima facie* case of anticipation since the Examiner fails to illustrate that the single prior art reference disclosure of Merchant includes the presence of each and every element recited by amended Claim 1 and as arranged in amended Claim 1. Lindemann, supra.

Accordingly, for at least the reasons indicated above, Applicants respectfully submit that amended Claim 1 is patentable over Merchant, as well as the references of record. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of amended Claim 1.

Regarding Claims 2-9, Claims 2-9, based on their dependency from Claim 1 and for at least the reasons described above, are also patentable over Merchant, as well as the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claims 2-9.

Regarding Claims 12-19, Claims 12-19, based on their dependency from Claim 11, are also patentable over Merchant, as well as the references of record. Therefore, Applicants

respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claims 12-19.

Regarding Claim 21, Claim 21 is amended to recite the following claim feature, which is neither disclosed nor suggested by Merchant:

blocked instruction detection logic to identify instructions blocked from execution by detected blocking conditions, and to enqueue the instructions onto the recirculation queue in one of a blocked state and an unblocked state, including a respective blocking condition of each instruction within the recirculation queue, wherein instructions having a transient blocking condition are enqueued onto the recirculation queue in the unblocked state. (Emphasis added.)

In contrast to the above-recited features of amended Claim 21, Applicants respectfully submit that the disclosure in Merchant is expressly limited to the handling of short latency instructions using replay loop 156, as shown in FIG. 1. As explicitly disclosed by Merchant:

For relatively short latency instructions like these (e.g., where there was a L0 cache miss and a L1 cache hit), only one or few iterations through the replay loop 156 will typically be required before the instruction will execute properly.

However, there may be one or more long latency instructions which will require many iterations through the replay loop 156 before finally executing properly. (col. 7, lines 9-16.) (Emphasis added.)

Accordingly, based on the cited passage above, Applicants respectfully submit that the delay provided through the replay loop 156 from staging queues E-F and A-D, as disclosed by Merchant, is sufficient for short latency instructions that require one or a few iterations through replay loop 156 before the instruction executes properly. (See, supra.) In contrast to the above-recited features of Claim 21, short latency instructions, as disclosed by Merchant, are not stored in replay queue 170 but in contrast are allowed to go through one or a few iterations through replay loop 156 before the instruction properly executes.

Hence, the disclosure in Merchant is explicitly contrary to the above-recited of amended Claim 21, which recites that instructions having a transient blocking condition are enqueued onto the recirculation queue in the unblocked state. Consequently, Applicants respectfully submit that the Examiner is prohibited from relying on Merchant as an anticipatory reference since Merchant fails to exactly disclose each and every element recited by amended Claim 21.

Therefore, Applicants respectfully submit that the Examiner fails to establish a *prima facie* case of anticipation since the Examiner fails to illustrate that the single prior art reference

disclosure of Merchant includes the presence of each and every element recited by amended Claim 21 and as arranged in amended Claim 21. Lindemann, supra.

Consequently, Applicants respectfully submit that Claim 21, as amended, is patentable over Merchant, as well as the references of record. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claim 21.

Regarding Claims 22-25, Claims 22-25, based on their dependency from Claim 21 and for at least the reasons described above, are also patentable over Merchant, as well as the references of record. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claims 22-25.

Regarding Claim 26, Claim 26 is amended to recite the following claim feature, which is neither disclosed, taught or suggested by Merchant:

blocked instruction detection logic to identify instructions blocked from execution by detected blocking conditions, and to enqueue the instructions onto the recirculation queue in one of a blocked state and an unblocked state, including a respective blocking condition of each instruction within the recirculation queue, wherein instructions having a transient blocking condition are enqueued onto the recirculation in the unblocked state. (Emphasis added.)

As indicated by the above-recited features of amended Claim 26, the above-recited feature of amended Claim 26 are analogous to the above-recited features of amended Claim 21. Accordingly, Applicants' arguments provided above with regard to the §102(b) rejection of Claim 21 as anticipated by Merchant equally apply to the Examiner's §102(b) rejection of Claim 26 as anticipated by Merchant.

Accordingly, for at least the reasons described above, Applicants respectfully submit that Applicants' amendments to Claim 26 prohibit the Examiner from establishing a *prima facie* case of anticipation since the amendments prohibit the Examiner from illustrating that the single prior art reference disclosure of Merchant includes the presence of each and every element recited by amended Claim 26 and as arranged in amended Claim 26. Id.

Consequently, for at least the reasons described above, Applicants respectfully submit that Claim 26, as amended, is patentable over Merchant, as well as the references of record. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of amended Claim 26.

Regarding Claims 27-30, Claims 27-30, based on their dependency from Claim 26 and for at least the reasons described above, are also patentable over Merchant, as well as the references of record. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §102(b) rejection of Claims 27-30.

III. Claims Rejected Under 35 U.S.C. §103

The Examiner rejects Claims 10 and 20 under 35 U.S.C. §103(a) as being unpatentable over Merchant. Applicants respectfully traverse this rejection.

Regarding Claims 10 and 20, Claims 10 and 20 depend from Claims 1 and 11. Applicants respectfully submit that amended Claims 1 and 11 are patentable over Merchant for at least the reasons provided above.

Consequently, Applicants respectfully submit that Claims 10 and 20, based on their dependency from amended Claims 1 and 11, respectively, are also patentable over Merchant. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 10 and 20.

CONCLUSION

In view of the foregoing, it is submitted that Claims 1-31 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

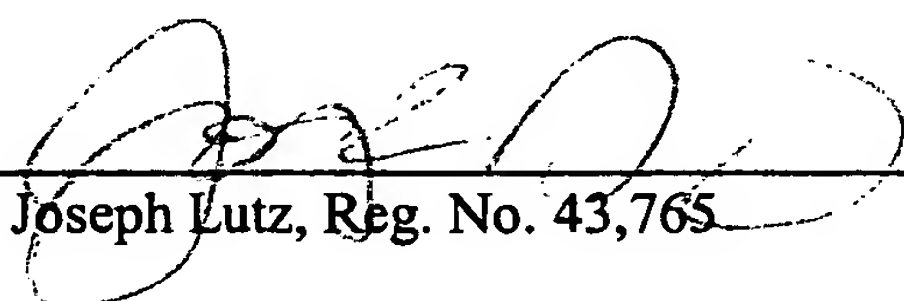
If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated : April 10, 2006

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CERTIFICATE OF MAILING:

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on April 10, 2006


Marilyn Bass

April 10, 2006